

R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Mai for the indication of allowable matter.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendment to the claims can be found in the drawings as originally filed, for example, on FIGS. 3-7 and in the specification as originally filed, for example, page 11, line 1 through page 12, line 15, on page 15, lines 1-10, and on page 20, line 14 through page 21, line 21. As such, no new matter has been introduced.

IN THE DRAWINGS

The objection to FIG. 4 has been obviated by appropriate amendment and should be withdrawn. A replacement drawing sheet is submitted herewith. Specifically, FIG. 4 has been amended for consistency with the specification. In particular, the reference numerals "150" and "152" have been transposed as suggested by the Examiner. Also, the reference label "REFL" in FIG. 4 has been replaced with "REFi". FIG. 2 has also been amended for consistency with the specification. In particular, the reference label "REF[o-n]" in FIG. 2 has been replaced with "REF[0-n]". Support for the amendments can be found in the specification as originally filed,

for example, on page 7, line 5 through page 9, line 9 and on page 16, lines 3-16. As such, no new matter is introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5-8, 10-19 and 21-26 under 35 U.S.C. §102(b) as being anticipated by Arimoto (U.S. Patent No. 5,798,976) is respectfully traversed and should be withdrawn.

Arimoto is directed to a semiconductor memory device with reduced current consumption in a data holding mode (Title).

In contrast, the presently claimed invention (claim 1) provides a method for reducing power consumption during background operations in a memory array with a plurality of sections comprising the step of controlling the background operations in each of the plurality of sections of the memory array in response to one or more control signals, where the background operations in each of the plurality of sections can be enabled independently of any other section. Claims 10 and 11 include similar limitations.

Arimoto does not disclose or suggest controlling the background operations in each of the plurality of sections of the memory array in response to one or more control signals, where the background operations in each of the plurality of sections can be enabled independently of any other section, as presently claimed. Specifically, Arimoto states that the array control circuit 12 can "select only one of the memory mats when the data holding mode is

designated" (column 5, lines 53-56 of Arimoto). Therefore, Arimoto does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-9 and 12-26 depend, either directly or indirectly, from claim 1 or claim 11 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

New claim 27 includes the allowable subject matter of originally presented claim 4. New claim 28 is believed to include the allowable subject matter of originally presented claim 9. New claims 29-31 depend, directly or indirectly, from either claim 1 or claim 11 which are believed to be allowable. As such, new claims 27-31 are fully patentable over the cited reference.

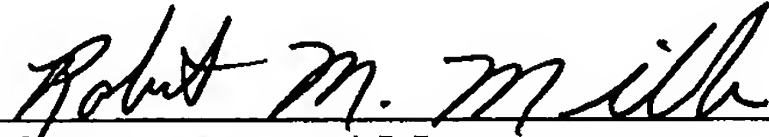
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office
Account No. 50-0541.

Respectfully submitted,

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Dated: June 4, 2004

Docket No.: 0325.00519c